NEC ELECTRON DEVICE

MOS DIGITAL INTEGRATED CIRCUIT
μPD2819C

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
CMOS LSI

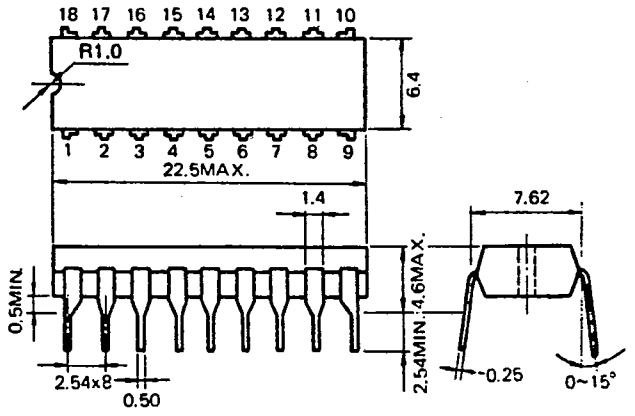
DESCRIPTION

The μPD2819C is a CMOS LSI for a Phase Locked Loop Frequency Synthesizer for Digital Tuning System.
The μPD2819C is packaged in a 18 pin plastic dual in-line package (DIP).

FEATURES

- Programmable divider : divided-by 20 to 7999 (BCD)
- Reference divider : f_{ref} = 10kHz, 9kHz, 5kHz, 4.5kHz, 2.5kHz, 1kHz
- Phase detector
- Reference oscillation circuit : 5.76MHz
- Filter amplifier : V_{DD2} = 20V (max.) open drain
- Serial data input : Numbers of lead wires = 3
- Two programmable divider inputs can be selected with program
- Data input terminal can withstand input voltage higher than supply voltage
  : $V_{IH2} = 0.7V_{DD1}$ to 15V
- Clock pulse output for a controller : 360kHz and 25Hz (open drain)
- Un-locked signal is detected as instant stop "IS" terminal
  : locked ... high level, un-locked ... pulsed wave
- High speed and low power consumption due to CMOS
- Single power supply
  : $V_{DD1} = 5 \pm 0.5$ volts
- Operating temperature $T_{opt} = -35$ to + 75 degrees centigrade

PACKAGE DIMENSIONS (Unit : mm)



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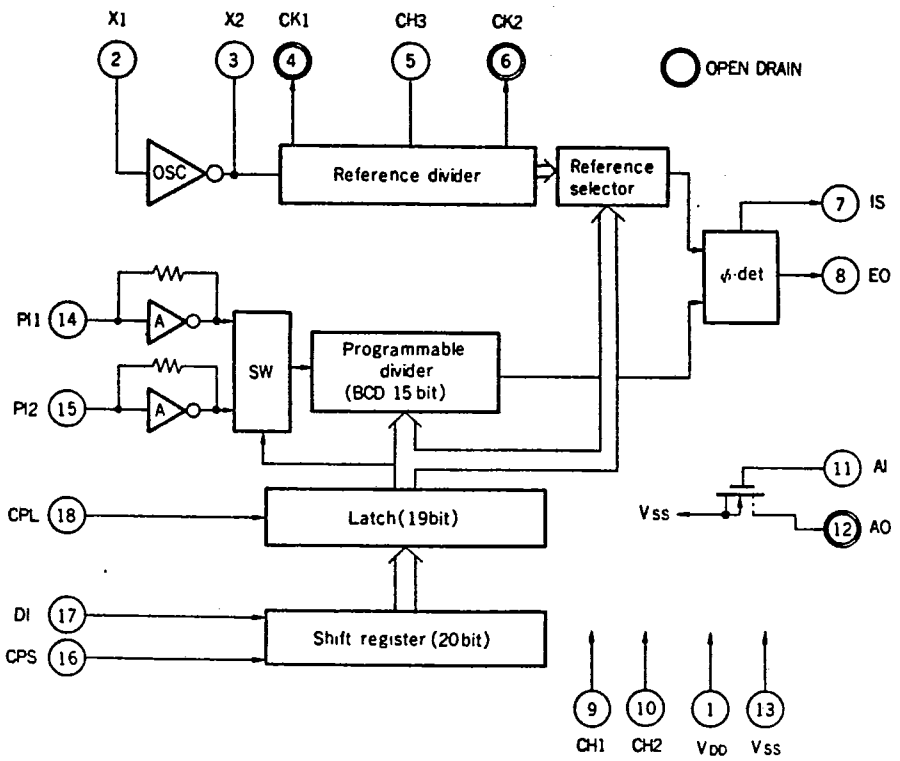
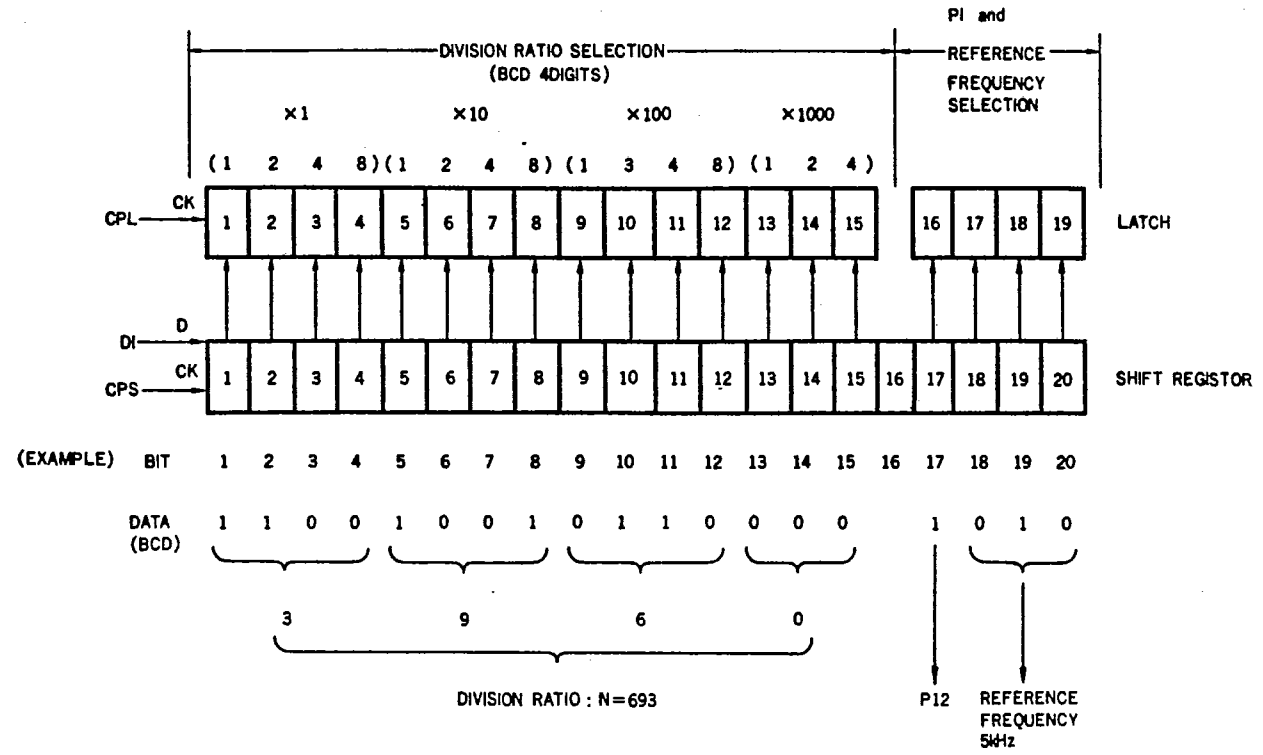
BLOCK DIAGRAM



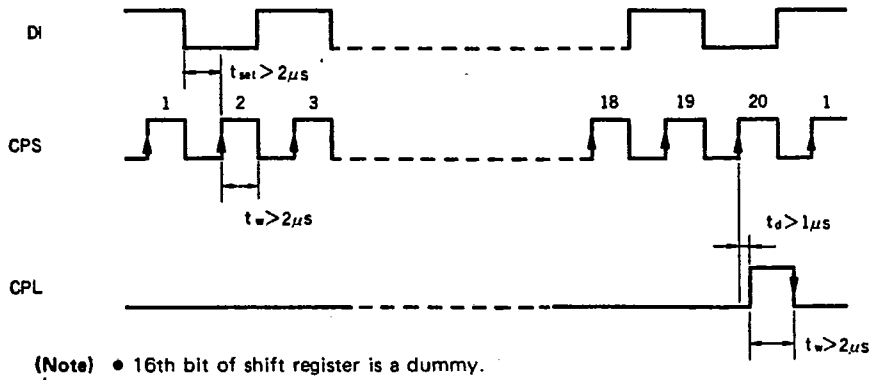
PIN CONNECTION

PIN#	SYMBOL	DESCRIPTION
1	V_{DD}	POWER SUPPLY (V_{DD} = 5 ±0.5V)
2	X1	X-tal OSCILLATOR (5.76MHz)
3	X2	
4	CK1	CLOCK OUTPUT (360kHz) OPEN DRAIN
5	CH3	CHECK TERMINAL (90kHz)
6	CK2	CLOCK OUTPUT (25Hz) OPEN DRAIN
7	IS	INSTANT STOP OUTPUT
8	EO	CHARGE PUMP OUTPUT (THREE STATE)
9	CH1	CHECK TERMINAL (REFERENCE FREQUNCY)
10	CH2	CHECK TERMINAL (PROGRAMMABLE DIVIDER OUTPUT)
11	AI	ACTIVE FILTER INPUT
12	AO	ACTIVE FILTER OUTPUT (OPEN DRAIN)
13	V_{SS}	GROUND
14	PI1	PROGRAMMABLE DIVIDER INPUT
15	PI2	PROGRAMMABLE DIVIDER INPUT
16	CPS	SHIFT REGISTER CLOCK INPUT
17	DI	SHIFT REGISTER DATA INPUT
18	CPL	LATCH CLOCK INPUT

INPUT PROGRAM DATA



DATA WAVE FORM (EXAMPLE)



(Note)
- 16th bit of shift register is a dummy.
- The data is shifted at positive edge of clock pulse (CPS).
- The data is latched at negative edge of latch pulse (CPL)

SELECTION OF PROGRAMMABLE DIVIDER INPUT AND REFERENCE FREQUENCY

17th bit	programmable divider input
0	PI1
1	PI2

reference frequency	18th bit	19th bit	20th bit
9	1	0	0
4.5	1	1	0
1	1	1	1
10	0	0	0
5	0	1	0
2.5	0	1	1

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage 1	V_{DD1}	−0.3 to +6.0	V	(V_{DD})
Supply Voltage 2	V_{DD2}	−0.3 to +20	V	(CK1, CK2, AO)
Input Voltage 1	V_{I1}	−0.3 to V_{DD1}	V	
Input Voltage 2	V_{I2}	−0.3 to +18	V	(CPL, CPS, DI)
Operating Temperature	T_{opt}	−35 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

ELECTRICAL CHARACTERISTICS (Ta = −35 to +75°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage 1	V_{DD1}	4.5	5.0	5.5	V	
High Level Input Voltage 1	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	all inputs except CPS, CPL, DI
High Level Input Voltage 2	V_{IH2}	$0.7V_{DD}$		15	V	CPS, CPL, DI
Low Level Input Voltage	V_{IL}	−0.3		$0.3V_{DD}$	V	all inputs except AI, PI1, PI2
High Level Output Voltage	V_{OH}	$0.7V_{DD}$		V_{DD}	V	all outputs, I_{OH} = −1.0mA
Low Level Output Voltage	V_{OL}	0		$0.3V_{DD}$	V	all outputs, I_{OL} = 1.0mA
High Level Input Current 1	I_{IH1}			1.0	μA	all inputs except AI, PI1, PI2
Low Level Input Current 1	I_{IL1}			−1.0	μA	all inputs except AI, PI1, PI2
High Level Input Current 2	I_{IH2}		1.0		nA	AI
Low Level Input Current 2	I_{IL2}		−1.0		nA	AI
Leak Current	I_L		1.0		nA	EO(floating)
Maximum Frequency Response	fdmax	5.76			MHz	X1−X2, DIVIDER, V_{DD} = 3.5V
	fpmax	7.2			MHz	PI1, PI2
Total Current	I_{DD}			5	mA	fin = 0, fd = 5.76MHz
A.C. Input Voltage	V_i	1.0			Vp-p	PI1, PI2

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