Power Devices

PCB Layout Thermal Design Guide

Thermal design is not only important in designing power circuits, but also an important element in designing the PCB. If an issue occurs after the design is completed, it requires more time and cost to make a modification. Therefore, it is necessary to perform the thermal design from the initial phase of the PCB design as well. This application note provides some key points on how to reduce thermal resistance in designing the PCB.

From here, we change the parameters of each PCB element and check changes in the thermal resistance. The measured value of each thermal resistance is listed for a 1-, 2-, or 4-layer PCB that complies with the JEDEC standard JESD51. Subsequently, after confirming consistency between the measured values as mentioned above and simulations, simulated values are listed for the PCB that are not in accordance with the JEDEC standard.

Since the thermal resistance values depend on the PCB material, layout, parts configuration, chassis shape, surrounding environment, and so on, they may not always be consistent with the values of actual equipment. Therefore, refer to trends of change in the thermal resistance, rather than the absolute values.

Copper foil area

Figure 1 shows the thermal resistance for the 1-layer board with varied copper foil areas. PCB layouts with different copper foil areas are shown in Figure 2. The thermal resistance is decreased as the copper foil area for heat dissipation is increased. However, the effect obtained may not be proportionate to the area if it is expanded beyond a certain extent. Figure 3 is a contour diagram showing that the area of the same temperature is increased as the distance from the heat source is increased. This indicates reduction in the heat dissipation effect.

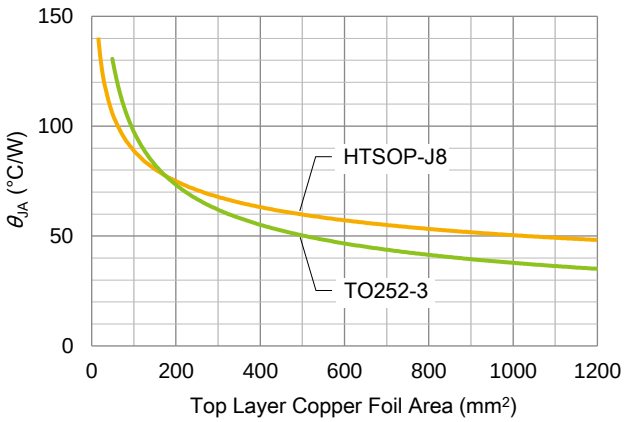

Figure 1. Thermal resistance with varied copper foil areas of the 1-layer board

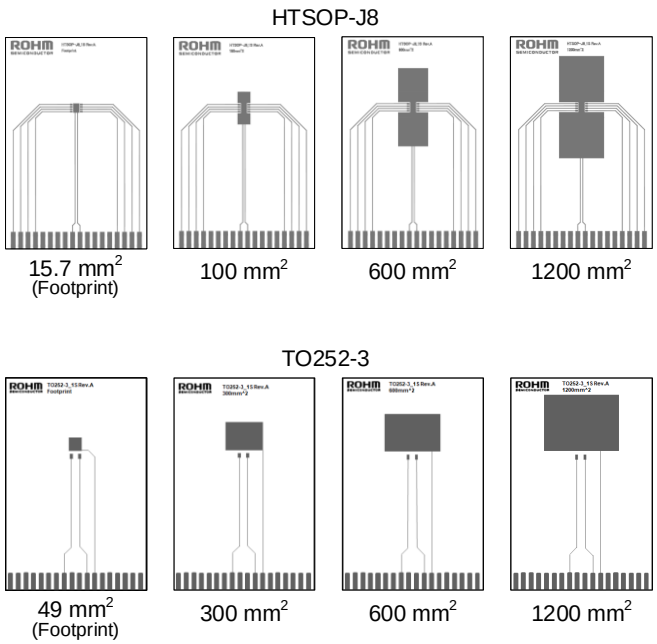

Figure 2. Layout of the 1-layer PCB

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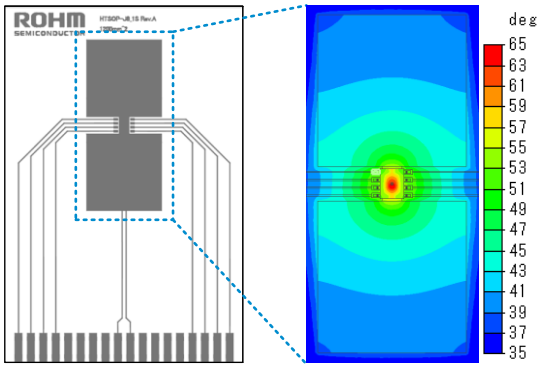


TO252-3

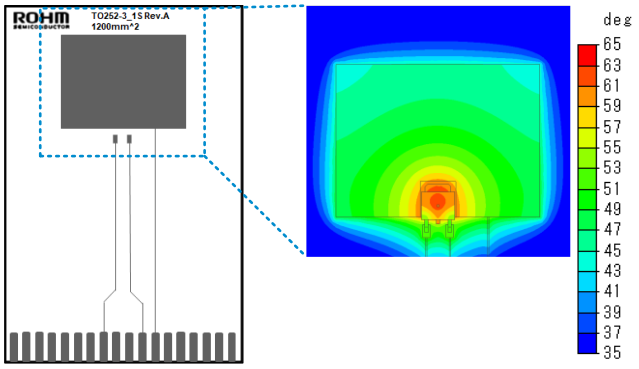


Figure 3. Contour diagram for the 1-layer board

Next, look at the change in thermal resistance for the multi-layer boards. Figure 4 shows the thermal resistance when the copper foil area is varied. Figure 5 shows the layouts of the 2- and 4-layer boards as typical examples. The layouts of the 6- and 8-layer boards correspond to that of the 4-layer board. As with the vertical structure shown in Figure 6, a thermal via penetrates from the top to bottom layers. Depending on the number of layers, the middle layers may or may not be connected with the thermal via. Refer to the respective diagrams.

As is the case for the change in thermal resistance for the 1-layer board, the thermal resistance for the multi-layer boards is decreased as the copper foil area for heat dissipation is increased. However, the effect obtained may not be proportionate to the area if it is expanded beyond a certain extent.

A significant difference in the thermal resistances is observed between the 2- and 4-layer boards. As can be seen in their vertical structures (Figure 6), the heat is transmitted from the heat source to the bottom layer through a via of 1.6 mm in length in the 2-layer board. In contrast, a large amount of heat is transmitted from the heat source to middle layer 1 over a shorter distance along the via in the 4-layer board. In other words, the shorter the distance from the heat source to the nearest copper foil for heat dissipation, the shorter the distance along the via, reducing the thermal resistance. Since this distance is even shorter in the 6- and 8-layer boards, the thermal resistance is decreased correspondingly.

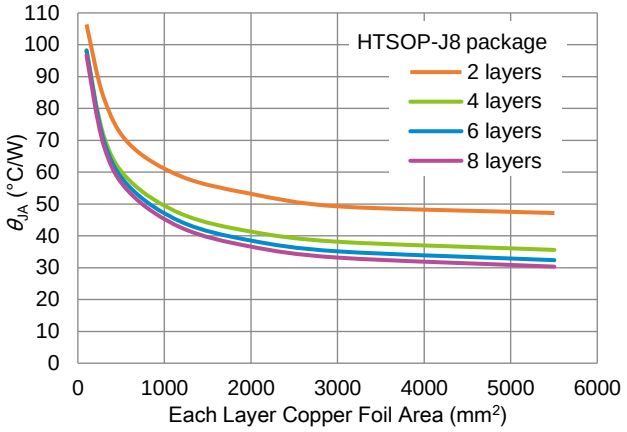
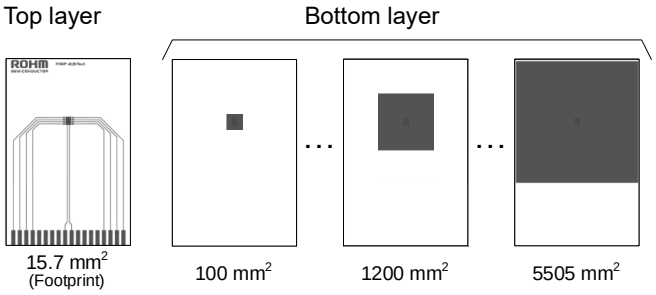


Figure 4. Thermal resistance for the multi-layer boards with varied copper foil areas except for the top layer

2-layer board



4-layer board

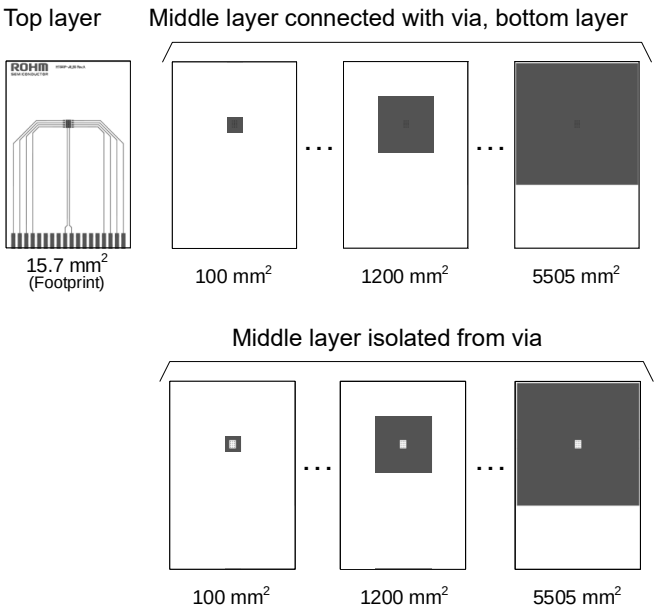
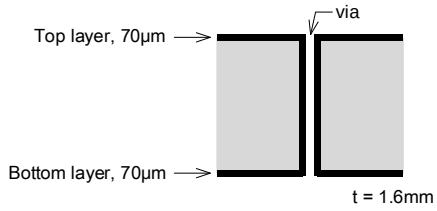
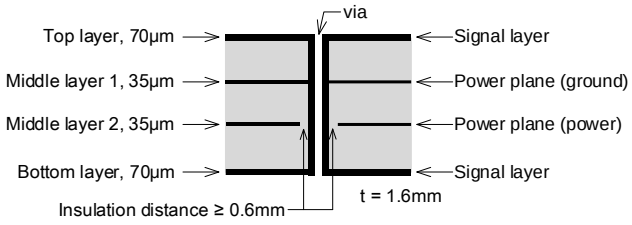


Figure 5. Layout of a multi-layer PCB

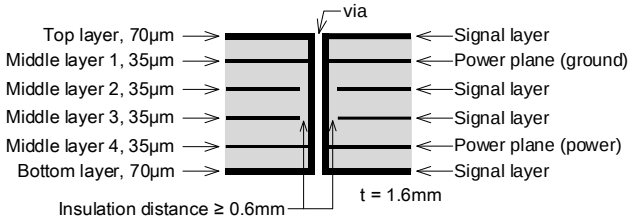
2-layer board



4-layer board



6-layer board



8-layer board

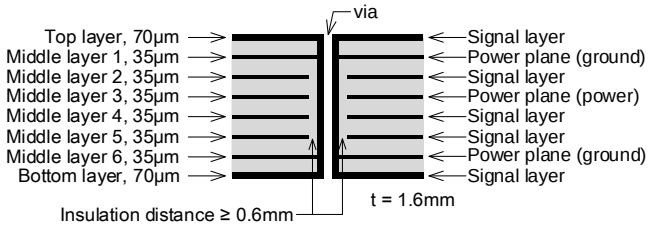


Figure 6. Vertical structure of a multi-layer PCB

Now look at how a large amount of heat is transmitted from the heat source to the nearest copper foil for heat dissipation. As shown in Figure 7, use a 4-layer board and lay out a large copper foil area of 5,505 mm^2 only for middle layers 1 and 2. However, middle layer 2 is not connected with the via. Figure 8 shows the thermal resistance when the copper foil area of the bottom layer is varied in this situation. As can be seen in the figure, if the heat can be sufficiently dissipated in a layer closer to the heat source, only a small effect can be obtained by securing a larger copper foil area in a layer farther from the heat source.

Thus, the thermal resistance can be efficiently reduced by preferentially increasing the copper foil area of layers closer to the heat source.

4-layer board

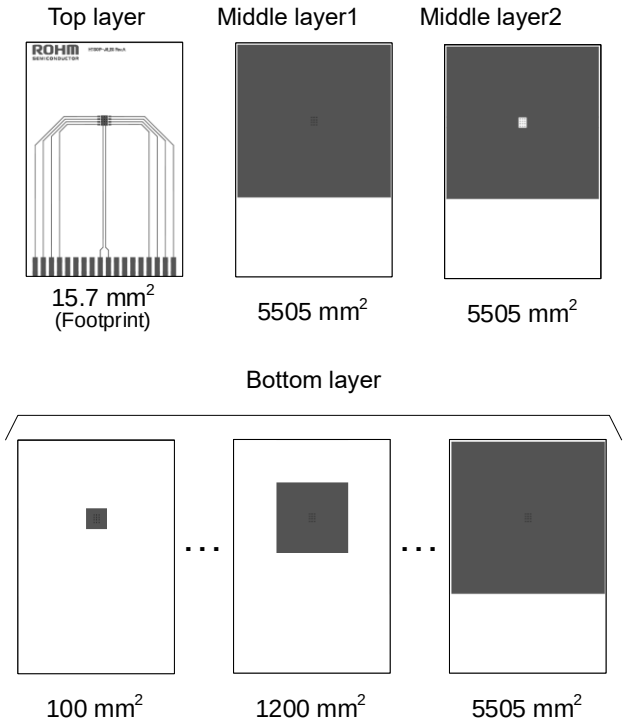


Figure 7. Layout of the 4-layer PCB with varied copper foil areas only for the bottom layer

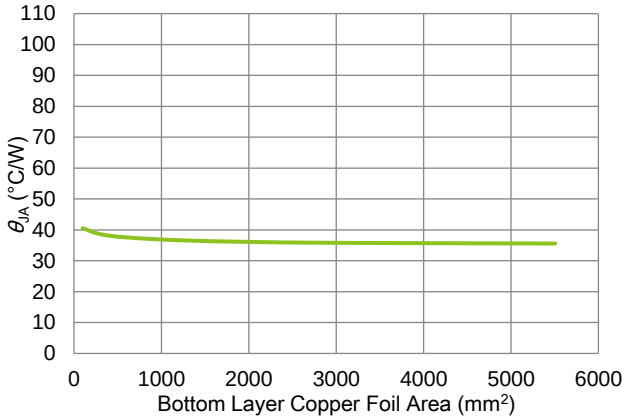


Figure 8. Thermal resistance when the copper foil area is varied only for the bottom layer in a case where the heat can be sufficiently dissipated in the layer close to the heat source in the 4-layer board

Board thickness

Figure 9 shows the thermal resistance for the 1-layer board with varied board thickness (refer to Figure 2 for the PCB). The vertical axis indicates the rate of change taking the thermal resistance with a board thickness of 1.6 mm as a reference (zero).

The thermal resistance tends to be smaller when the board thickness is larger. In the 1-layer board, the heat cannot be efficiently dissipated through the vertical thermal conduction, because the air layer on the bottom surface has a small thermal conductivity. Therefore, the horizontal thermal conduction takes precedence. To reduce the horizontal thermal resistance, increase the board thickness. Figure 10 shows how the heat is conducted with varied board thickness. This indicates that the heat is conducted farther in a thicker board.

In Figure 9, the change in thermal resistance against the board thickness is reduced in a larger copper foil area of the top layer. This is because the precedence of the thermal conduction to the copper foil is increased as the copper foil area is increased, reducing the relative influence of the board thickness on the thermal resistance.

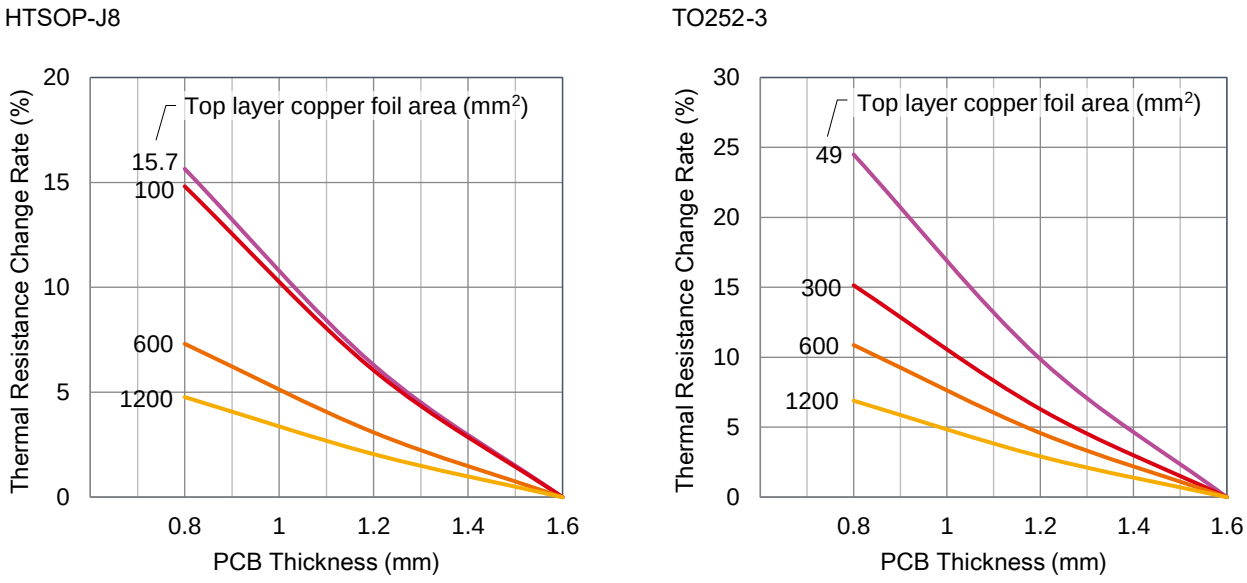


Figure 9. Thermal resistance for the 1-layer board with varied board thickness

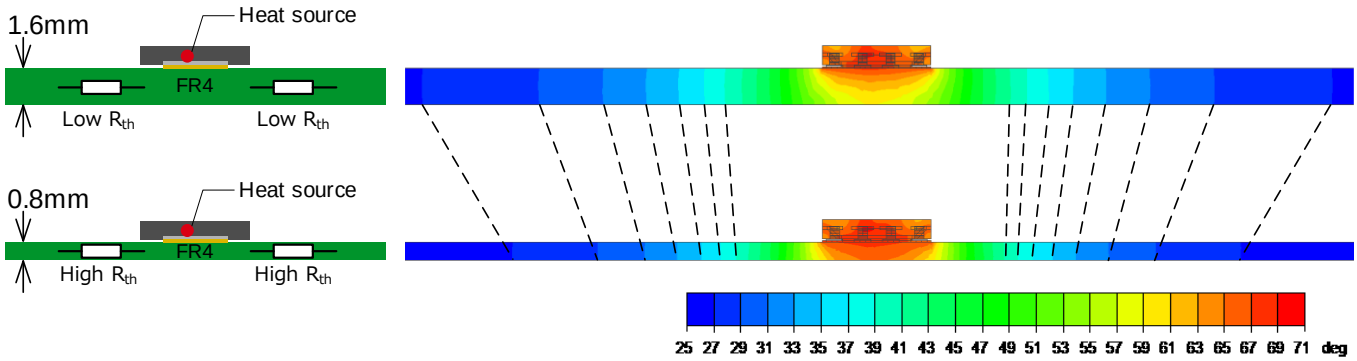


Figure 10. Thermal conduction with varied board thickness in the 1-layer board
(HTSOP-J8, copper foil area of the top layer is 15.7 mm², both heat sources at the same temperature)

Figure 11 shows the thermal resistance for the 2-layer board layout with varied board thickness, where the heat source is connected to the copper foil of the bottom layer through a thermal via (refer to Figures 5 and 6 for the PCB). The vertical axis indicates the rate of change taking the thermal resistance with a board thickness of 1.6 mm as a reference.

As is the case for the 1-layer board, the thermal resistance tends to be smaller when the board thickness is larger, because the thermal conduction to the board is relatively larger with a smaller copper foil area.

As the copper foil area is increased, the thermal conduction to the copper foil through the via is relatively increased. Therefore, thermal resistance tends to be smaller when the distance along the via is shorter (the thermal resistance along the via is lower), i.e., the board thickness is smaller.

The horizontal thermal conduction takes precedence with a smaller copper foil area, whereas the vertical thermal conduction takes precedence with a larger copper foil area. This boundary depends on the PCB conditions.

Figure 12 shows how the heat is conducted with varied board thickness. This indicates that the vertical thermal conduction is more effective with a smaller board thickness if a sufficient copper foil area for heat dissipation is available in the bottom layer.

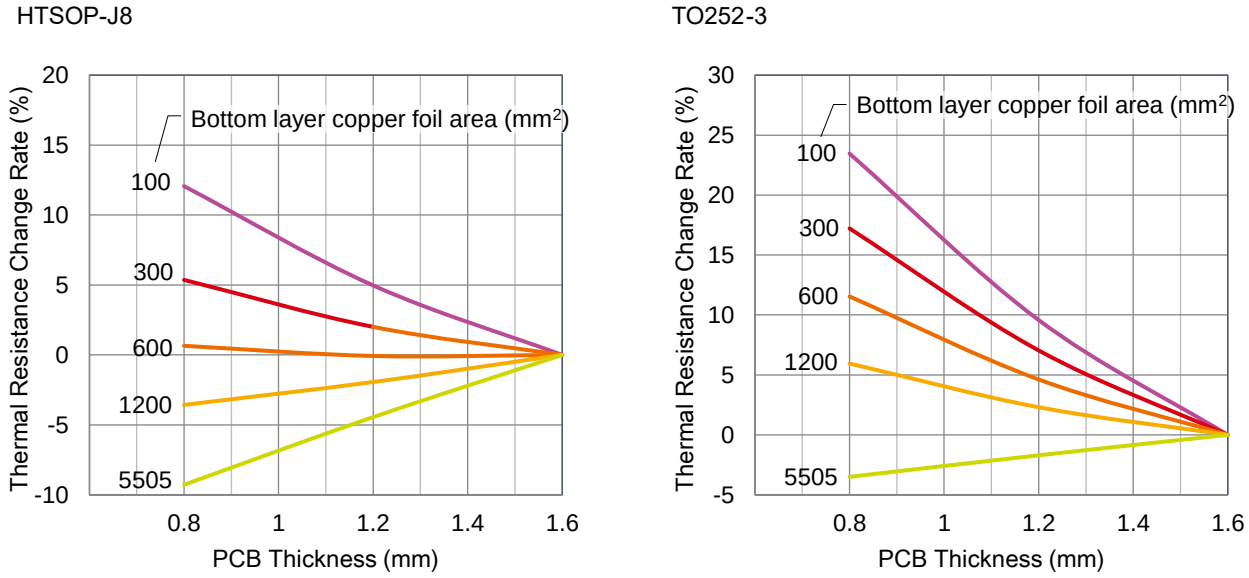


Figure 11. Thermal resistance for the 2-layer board with varied board thickness

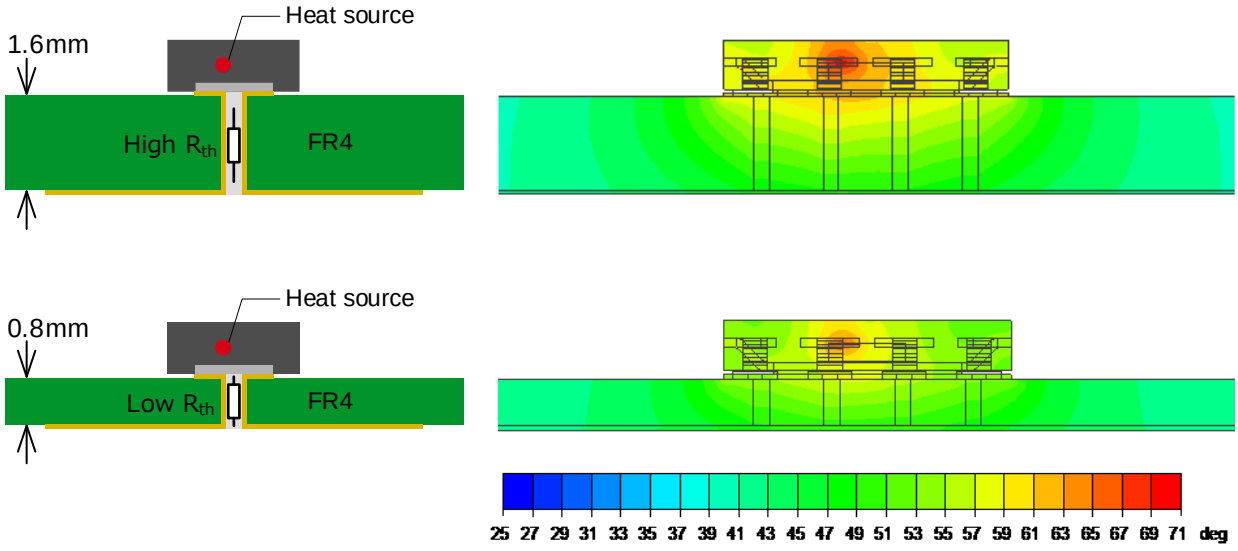


Figure 12. Thermal conduction with varied board thickness in the 2-layer board
(HTSOP-J8, copper foil area of the bottom layer is 5,505 mm², both heat sources with the same power loss)

Number of layers

Figure 13 shows the thermal resistance with varied numbers of layers (refer to Figures 5 and 6 for the PCB). The thermal resistance tends to be lower with a larger number of layers. This reduction in the thermal resistance is due to the increase in the copper foil area for the thermal conduction and, as described in the section for “Copper foil area”, the decrease in the distance from the heat source to the nearest middle layer copper foil (plane) as the number of layers is increased with the same board thickness based on the vertical structure (Figure 6).

Table 1 shows typical assignments of the layers. From the EMI aspect, the plane layers with a low electric impedance (ground or power supply) are generally placed adjacent to all the wiring layers. This configuration is also very effective for the thermal design, because the heat can be efficiently conducted from the heat source on the top layer (L1 here) to plane L2, which is the middle layer directly below the top layer.

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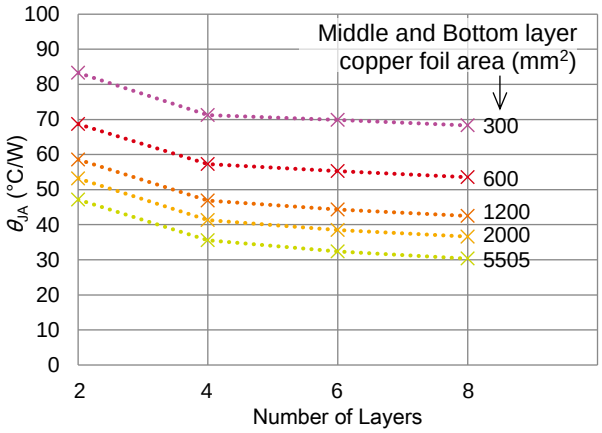


TO252-3

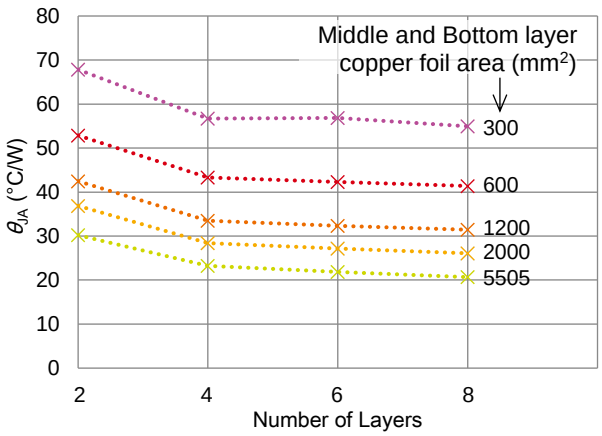


Figure 13. Thermal resistance with varied numbers of layers

Table 1. Typical layer assignments

Layer	Layer assignment			
	2-layer PCB	4-layer PCB	6-layer PCB	8-layer PCB
L1 (Top)	Wiring	Wiring	Wiring	Wiring
L2	Wiring	Ground plane	Ground plane	Ground plane
L3		Power plane	Wiring	Wiring
L4		Wiring	Wiring	Power plane
L5			Power plane	Wiring
L6			Wiring	Wiring
L7				Ground Plane
L8				Wiring

For example, the thermal conduction is not optimum even with an 8-layer board if the heat source on the top layer is not connected with the middle layers through the via and a large copper foil area is provided in the bottom layer (L8 here), because the vertical thermal resistance along the via is increased. In this case, the thermal resistance can be reduced to a certain extent by increasing the copper foil thickness of the bottom layer.

In the multi-layer boards, the thermal resistance can be efficiently lowered by placing a larger copper foil area for heat dissipation on the same layer as the heat source or the adjacent layer.

Figure 14 shows the thermal resistance for the 8-layer board when a heat dissipation plane is placed only on a certain layer. It can be seen that the thermal resistance is higher as the distance from the heat source on L1 is increased.

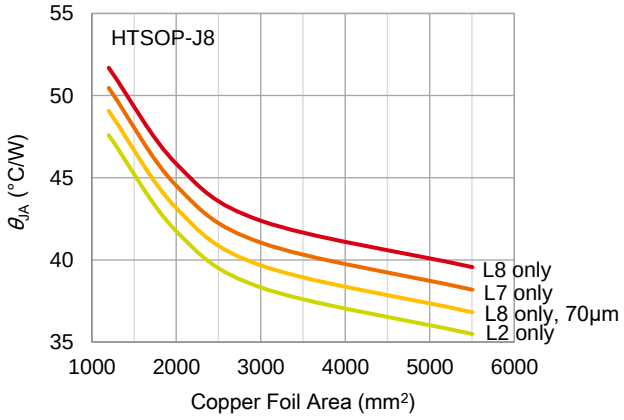


Figure 14. Change in thermal resistance for the 8-layer board when a heat dissipation plane is placed only on a certain layer (copper foil thickness is 35 µm unless otherwise specified)

Copper foil thickness

Figure 15 shows the trend in the thermal resistance with varied copper foil thickness. The thicker the copper foil, the lower the thermal resistance. This is because the thermal resistance of the copper foil itself, which provides the heat conduction path, is decreased.

In this figure, the variation rate is shown taking the thermal resistance with the copper foil thickness of 70 µm as a reference (zero). The copper foil thickness of the top and bottom layers is varied, while that of the middle layers is fixed at 35 µm. The variation rate depends on the number of layers in the PCB. However, this should be considered as only an example because it depends on the PCB configuration, such as the copper foil area.

The PCB layouts for this figure are shown in Figures 2, 5, and 6. The copper foil area is footprint size only for the top layer and 5,505 mm^2 for the middle and bottom layers.

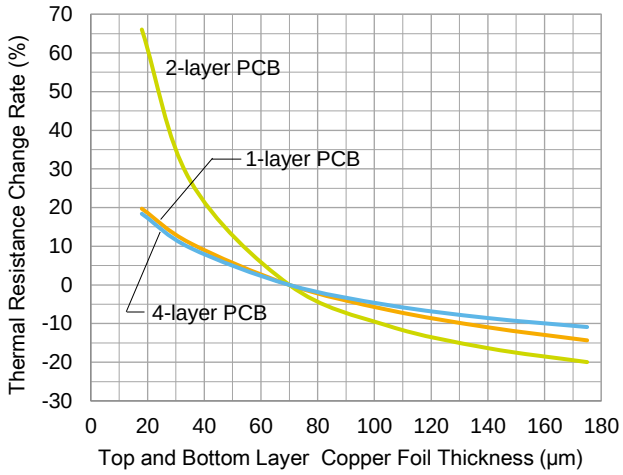
The effect of the copper foil thickness appears to be small for the 1-layer PCB, because of its small copper foil area with footprint size only. Figure 16 shows the result of increasing the copper foil area to 1,200 mm^2. It can be seen that the relative influence of the copper foil thickness is increased as the thermal conduction to the copper foil is increased.

A larger variation rate in the 2-layer PCB is a result of the larger relative influence of the copper foil thickness, because the main thermal conduction path is the copper foil of the bottom layer.

In the 4-layer PCB, the relative influence of the copper foil thickness of the bottom layer appears to be smaller, because the thermal conduction to the middle layers is larger.

In any case, the thicker the copper foil, the lower the thermal resistance.

HTSOP-J8



TO252-3

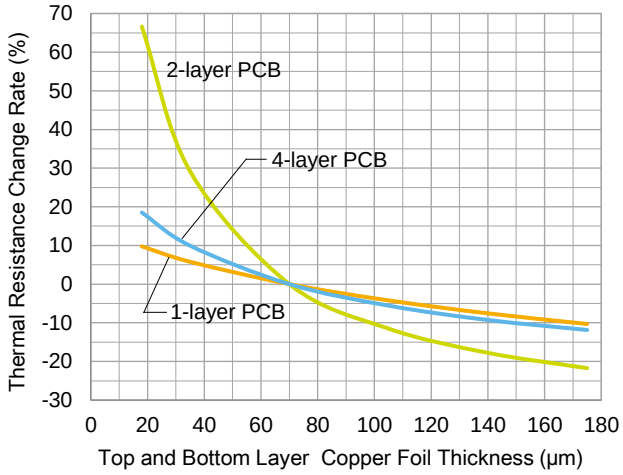


Figure 15. Thermal resistance with varied copper foil thickness

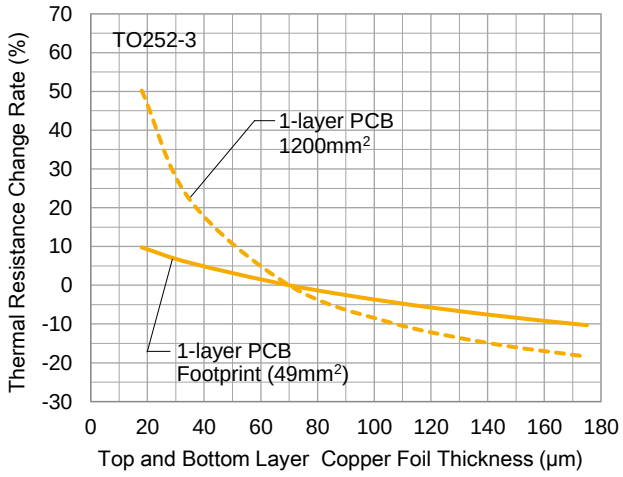


Figure 16. Rate of variation in the thermal resistance when the copper foil area is 1,200 mm^2 in the 1-layer PCB of TO252-3

Thermal via

Figure 17 shows the change in thermal resistance with the number of thermal vias in the PCB on which the HTSOP-J8 package is mounted. The larger the number of vias, the lower the thermal resistance. However, it can be seen that only one via has a large effect.

If a via is placed directly under the exposed pad, solder may be sucked into the via during the reflow process, reducing the fusion ratio. Countermeasures against this issue include designing stencils (metal masks) away from the vias and placing the vias on the periphery and away from the exposed pad. Figure 18 shows the changes in thermal resistance with the respective countermeasures. When the stencil is engineered (I), the thermal resistance is only slightly increased. However, when the vias are placed around the exposed pad (J), the thermal resistance component of the copper foil is added because the heat is first transmitted through the copper foil and then reaches the via. Therefore, since the effect of thermal vias is decreased as they are separated from the heat source, place them directly under the heat source as much as possible.

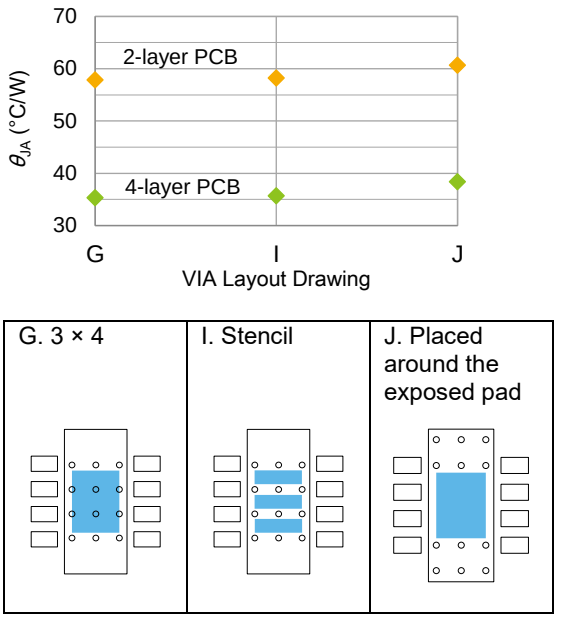


Figure 18. Change in the thermal resistance with the countermeasures against solder being sucked into the vias

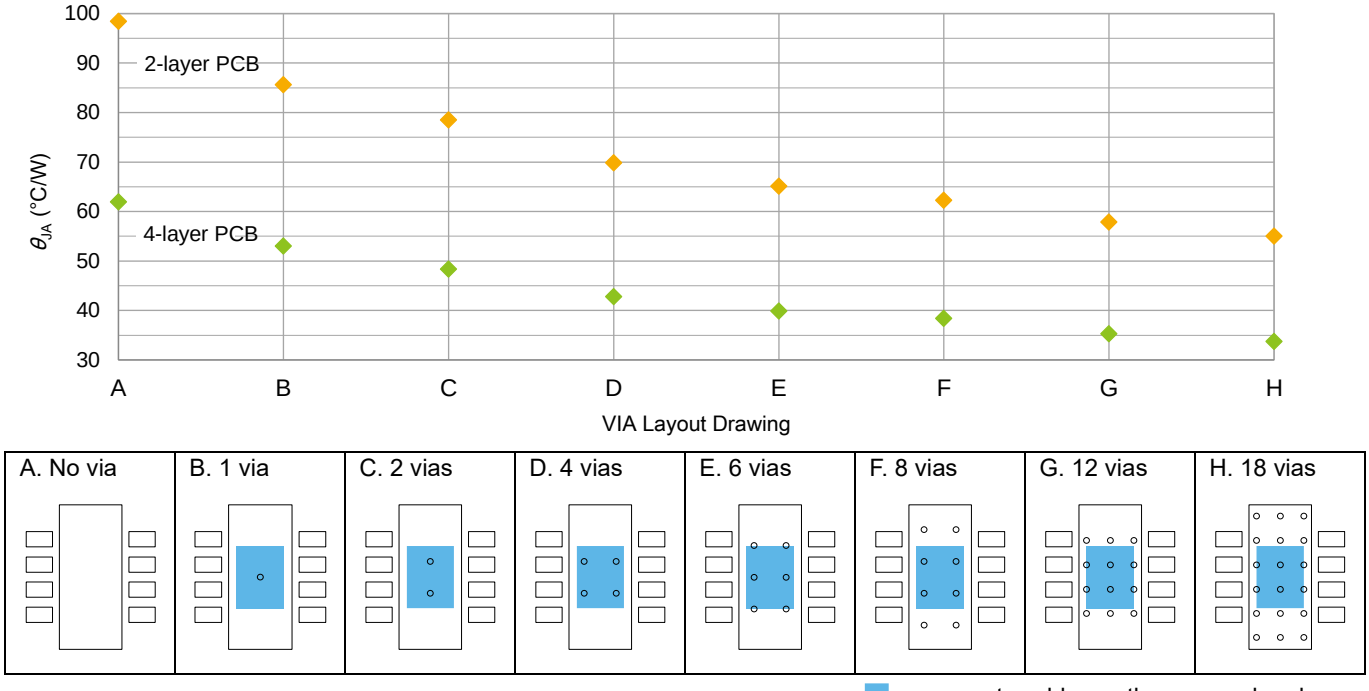


Figure 17. Change in the thermal resistance with the number of vias
HTSOP-J8 package, via diameter 0.3 mm

Figure 19 shows the thermal resistance with varied via diameters. The larger the via diameter, the lower the thermal resistance. This is because of a decrease in the thermal resistance of the via itself, which provides the heat conduction path.

In this example, the vias are placed on the same positions for different via diameters to check their effect. In reality, vias with a smaller diameter can be placed at narrower pitches. Therefore, the actual thermal resistance for the via diameters of 0.3 mm and 0.5 mm is lower compared with this example. Layout K (0.3 mm) corresponds to layout J on the previous page.

If vias are placed in the solder area directly under the exposed pad or FIN, the recommended via diameter is 0.3 mm or less to prevent solder from being sucked into vias.

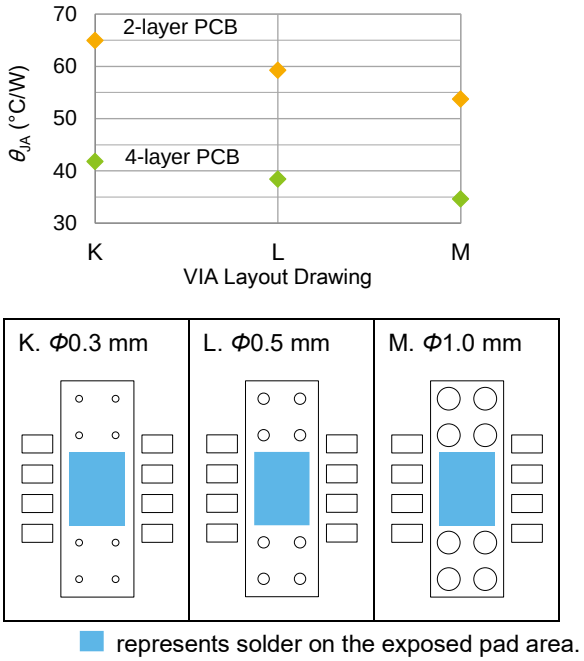
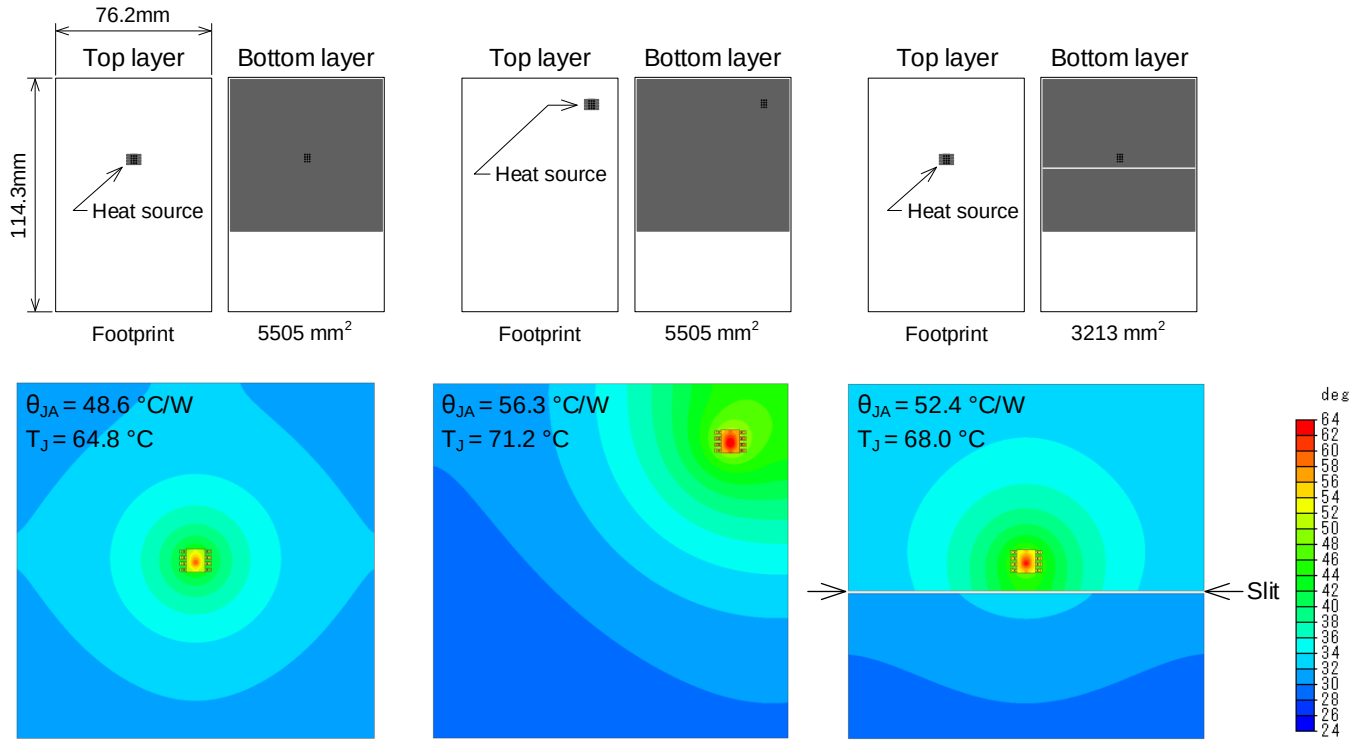


Figure 19. Thermal resistance with varied via diameters

Position of heat source

Figure 20 shows the change in thermal resistance with different positions of the heat source on the board. In case A, the heat source is placed on the center of the board. Since the heat is conducted in all directions, the thermal resistance is lowest. In case B, the heat source is placed on one end of the board. Since the volume for thermal conduction is decreased, the thermal resistance is higher. In case C, the copper foil plane, which is the main destination of the thermal conduction, is divided with a slit. It is possible that slits are formed in the ground plane as a countermeasure against the EMI or noise, separately providing the ground for each function block. In such cases, the copper foil area of the main destination of the thermal conduction is decreased. However, since there are other heat dissipation paths, such as the board (FR4), the increase in the thermal resistance is smaller compared with the case where the heat source is placed on one end.

Since there are many parts in the actual equipment, it is difficult to secure a large copper foil area for one heat source. However, it is important to intentionally lay out the heat source on the center so that the copper foil area can be evenly secured around 360°.



A. Placed on the center

B. Placed on one end

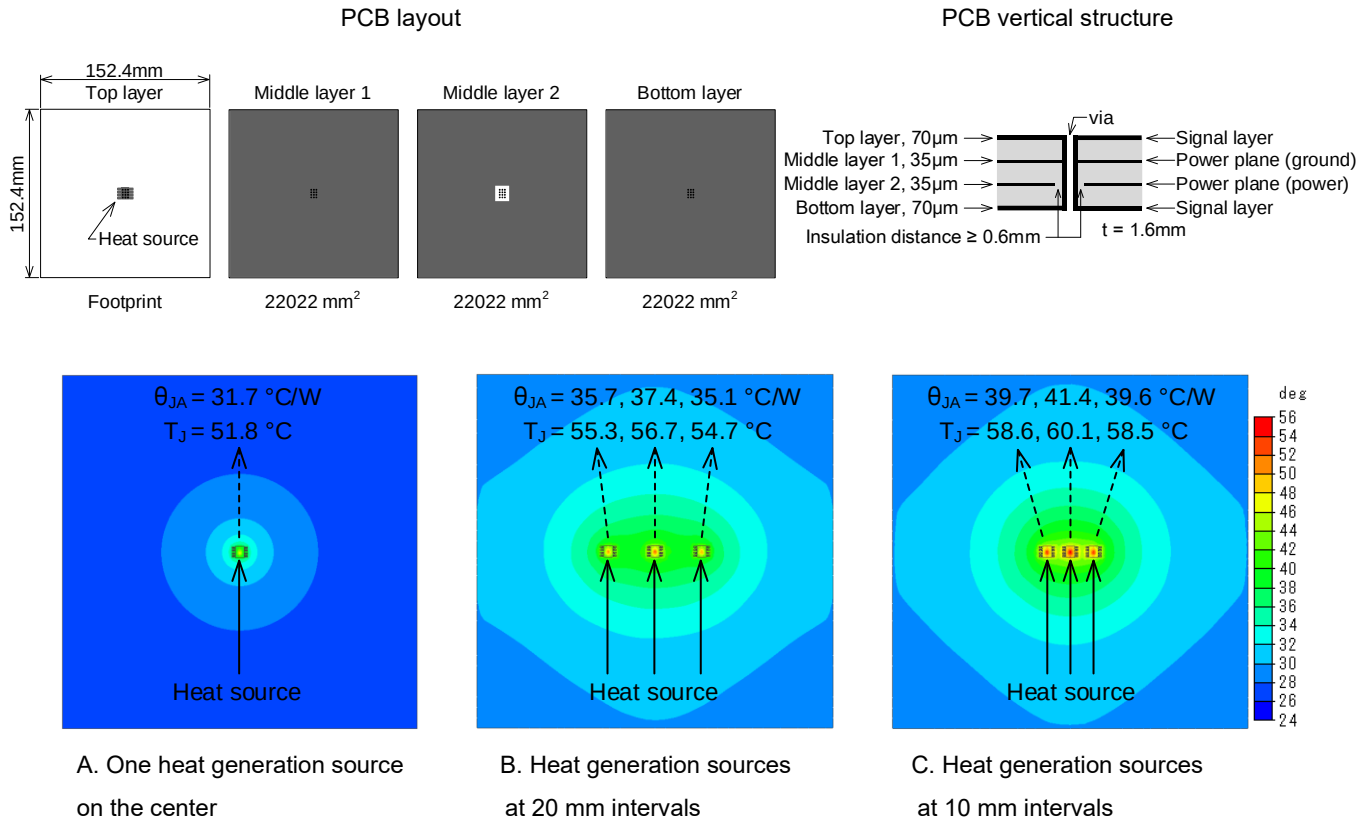
C. Ground plane divided with slit

Figure 20. Change in the thermal resistance due to difference in the positions of the heat source
Contour diagram viewing the copper foil of the bottom layer in the 2-layer board from the top
The same power loss for the heat sources

Neighboring heat sources

Figure 21 shows the change in thermal resistance when heat sources are closely placed. In this example, three heat sources with the same power loss are closely placed in B and C. The thermal resistance is higher compared with A, where only one heat source is placed. This is because each device experiences thermal interference, increasing the ambient temperature around the devices. The shorter the distance between the heat sources, the stronger the influence they experience.

Like this example, even when the temperature increase is below the design target value after the thermal design for each heat source, the thermal interference phenomenon should be considered in the thermal design if the three heat sources operate simultaneously and are thermally influenced by each other. Such cases may occur in power supplies with multi-channel output, LED drivers, motor drivers, etc.



A. One heat generation source on the center

B. Heat generation sources at 20 mm intervals

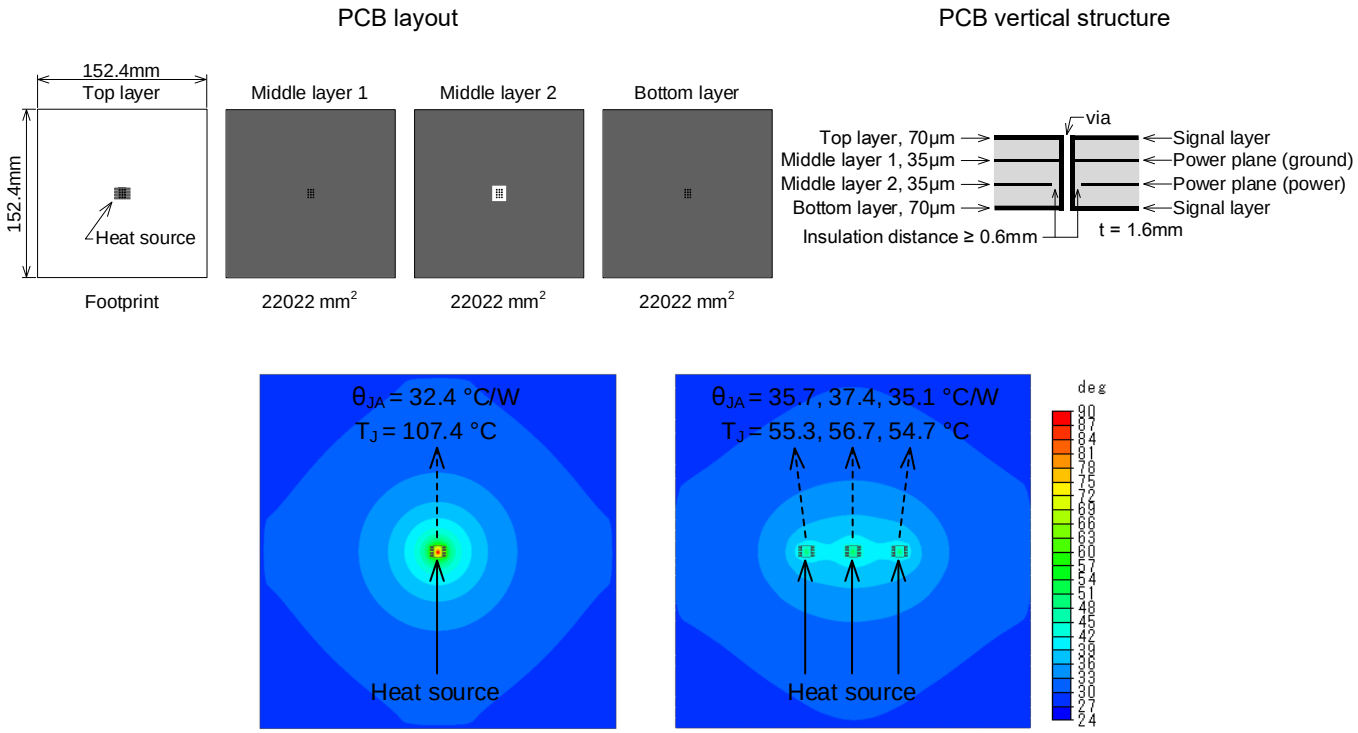
C. Heat generation sources at 10 mm intervals

Figure 21. Change in the thermal resistance when heat sources are closely placed
Contour diagram viewing the 4-layer board from the top
The same power loss for the heat sources

Distributed heat sources

Figure 22 shows the change in thermal resistance if the heat sources are distributed. In case A, the power loss occurs in one device and the junction temperature is 107.4°C. In case B, the power loss in case A is evenly distributed to three devices. Although the thermal interference occurs between the devices, it can be seen that the temperature increase is mitigated by distributing the heat sources. This is because the thermal resistance is decreased as the thermal conduction area is increased.

Thus, distribution of the heat sources (power loss) is an effective measure to decrease the temperature of each device. An IC package is taken as an example here. However, the same effect is obtained for passive elements such as resistors.



A. Power loss in one device B. Power is distributed to three devices

Figure 22. Change in the thermal resistance with distributed heat sources
Contour diagram viewing the 4-layer board from the top
Total power loss is the same for the heat sources on the board.

Consideration of passive components vulnerable to high temperature

It is known that electrolytic solutions in electrolytic capacitors tend to evaporate at higher temperatures, reducing the life of the capacitors. Therefore, it is necessary to decrease excessive temperatures in order to extend the life of components vulnerable to high temperatures. There are three paths from a heat source to passive components: thermal conduction, convection (heat transmission), and heat radiation. For the convection (heat transmission), ventilate the chassis to decrease the inside temperature. For the heat radiation, separate the components from the heat source or provide a heat insulating plate to shield the components from heat. For the thermal conduction, the heat is conducted mainly through copper wiring. Therefore, separate the components from the heat source or minimize the width of the copper wiring.

Figure 23 shows an LDO circuit as an example. However, in some cases, an electrolytic capacitor must be placed near a heat source device to achieve certain electrical characteristics. For three-terminal LDO, many pin layouts, such as the TO252 package, use FIN for heat dissipation in combination with a ground terminal. Placing electrolytic capacitors C_1 and C_2 near the device results in the layout as shown in Figure 24. Since the copper foil in the heat dissipation area and the ground wiring are shared, the heat from FIN for heat dissipation is conducted through the wide copper foil to the capacitors as shown in Figure 25. The temperature at the capacitor terminals is 57°C.

As a countermeasure, minimize the thermal conduction by reducing the wiring width to the minimum current capacity tolerance and place the capacitors at the same distance from the heat source, as shown in Figure 26. Figure 27 is the result, showing a decrease in the capacitor terminal temperature to 44°C.

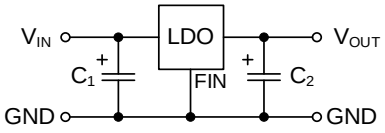


Figure 23. LDO circuit diagram

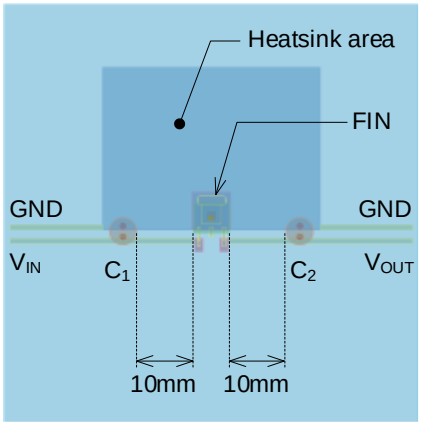


Figure 24. PCB layout in which the capacitors are placed in the heat dissipation area

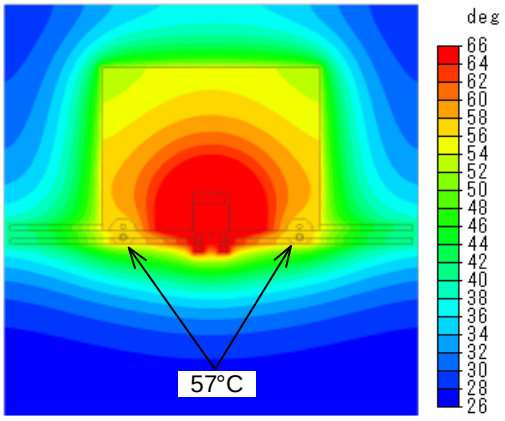


Figure 25. Contour diagram when the capacitors are placed in the heat dissipation area

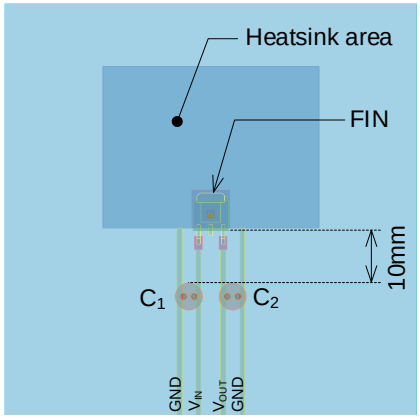


Figure 26. PCB layout in which the capacitors are placed away from the heat dissipation area

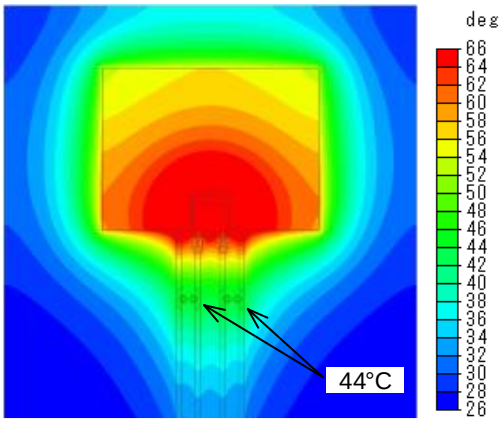


Figure 27. Contour diagram when the capacitors are placed away from the heat dissipation area

This is because the thermal conduction over the same distance becomes more difficult due to higher thermal resistance for the board (FR4) compared with the copper foil.

As described above, a layout focusing only on the electrical characteristics may cause a thermal issue. Therefore, it is necessary to consider the positional relation of the devices that act as heat sources and the devices vulnerable to high temperature.

For AC-DC converters and the like, the AC ripple current is smoothed with an electrolytic capacitor. However, a large ripple current and the internal resistance of the capacitor generate a power loss, causing self-heating of the capacitor. In such cases, contrary to the layout described above, increase the wiring area and allow the heat to be conducted to the wiring.

Temperature increase of copper foil wiring

For a conductor (copper foil wiring) through which a large current flows, it is necessary to determine the minimum width and thickness based on the required current capacity and the maximum tolerance for increase in the conductor temperature. Neglecting this may cause a temperature increase, deteriorating the PCB or increasing the ambient temperature.

Refer to the following figures for the minimum width and thickness of conductors. These figures are produced based on the approximations and figures published in “IPC-2221A, Generic Standard on Printed Board Design” with the units converted to the metric system.

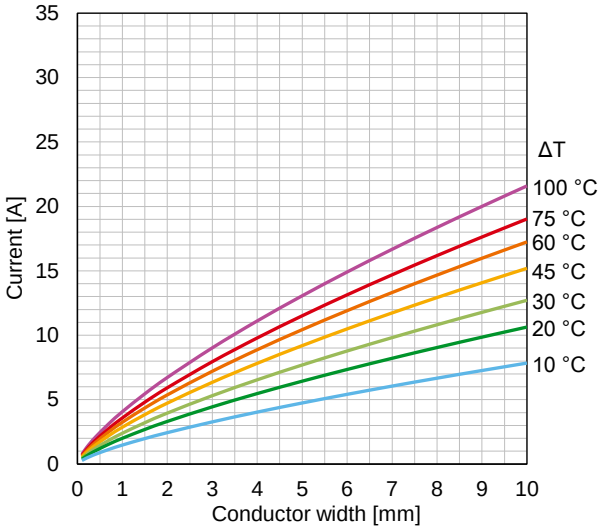


Figure 28. Temperature increase due to the conductor width and current.
1- and 2-layer PCB and outer layers of multi-layer PCB.
Conductor thickness 18 µm.

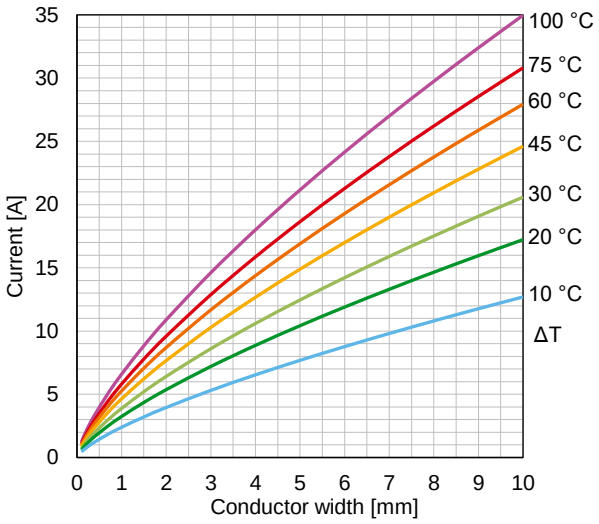


Figure 29. Temperature increase due to the conductor width and current.
1- and 2-layer PCB and outer layers of multi-layer PCB.
Conductor thickness 35 µm.

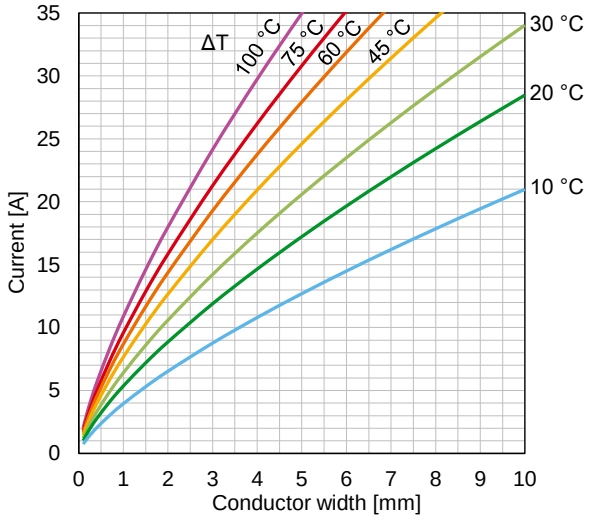


Figure 30. Temperature increase due to the conductor width and current.
1- and 2-layer PCB and outer layers of multi-layer PCB.
Conductor thickness 70 µm.

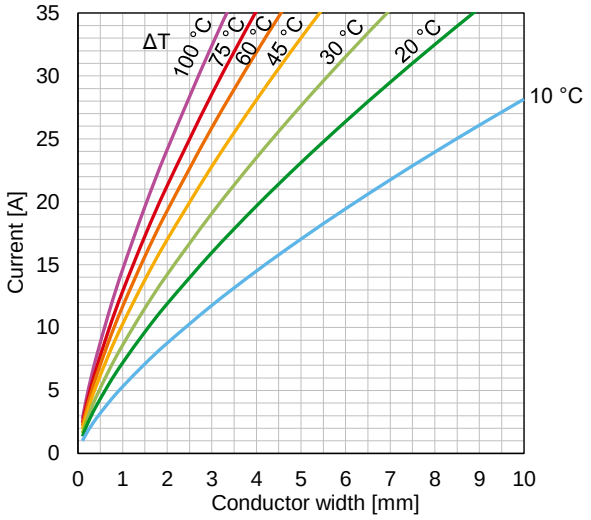


Figure 31. Temperature increase due to the conductor width and current.
1- and 2-layer PCB and outer layers of multi-layer PCB.
Conductor thickness 105 µm.

Figures 28 to 31 show the temperature increase applied to the 1- and 2-layer PCB and the outer layers of the multi-layer PCB for each conductor thickness. Similarly, Figures 32 to 35 show the temperature increase applied to the middle layers of the multi-layer PCB.

In the same way for the thermal resistance of the semiconductor packages, the values of increases in the copper wiring temperature depend on the PCB material, layout, parts configuration, chassis shape, surrounding environment, and so on. Therefore, use these figures as a rough guide.

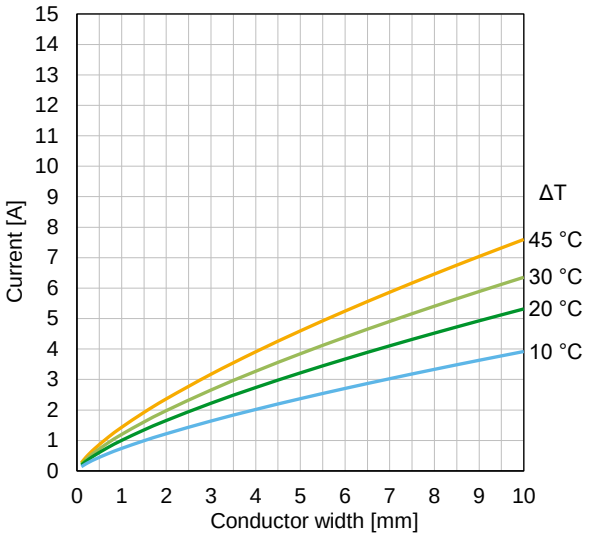


Figure 32. Temperature increase due to the conductor width and current.
Middle layers of multi-layer PCB
Conductor thickness 18 µm.

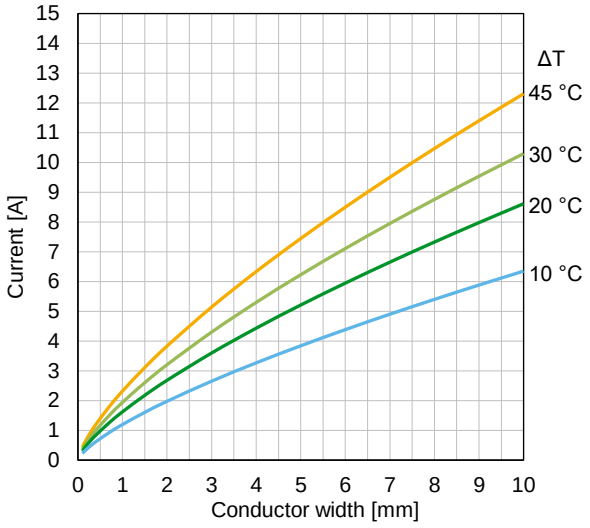


Figure 33. Temperature increase due to the conductor width and current.
Middle layers of multi-layer PCB
Conductor thickness 35 µm.

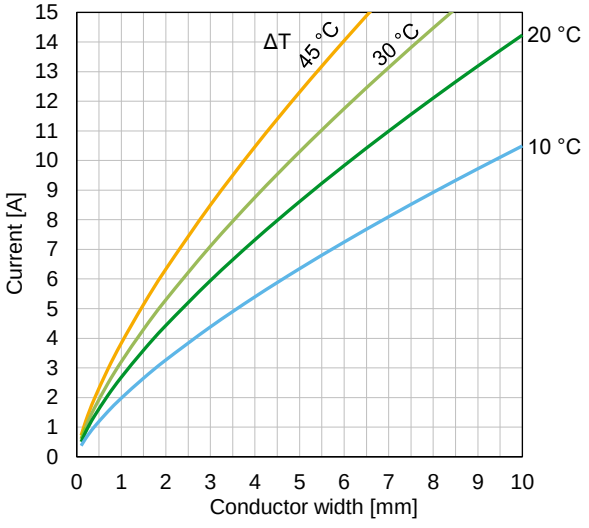


Figure 34. Temperature increase due to the conductor width and current.
Middle layers of multi-layer PCB
Conductor thickness 70 µm.

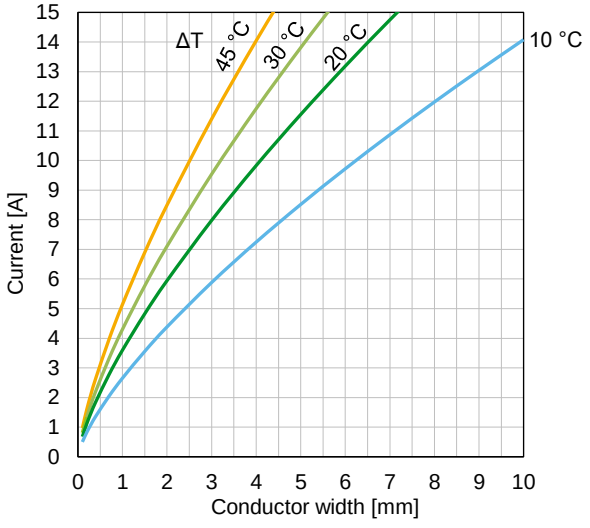


Figure 35. Temperature increase due to the conductor width and current.
Middle layers of multi-layer PCB
Conductor thickness 105 µm.

Summary of key points for reducing the thermal resistance

Copper foil area

- The larger the copper foil area, the lower the thermal resistance.
- Select an appropriate size of the copper foil area. If the copper foil area is expanded more than necessary, the thermal conduction efficiency is decreased as the distance from the heat source is increased, and the effect obtained may not be proportionate to the area.
- In the multi-layer boards, the thermal resistance can be efficiently reduced by preferentially increasing the copper foil area of layers closer to the heat source.

Board thickness

- In the 1-layer boards, since the horizontal thermal conduction takes precedence, increasing the board thickness reduces the thermal resistance.
- In the multi-layer boards, the horizontal thermal conduction takes precedence if the copper foil area for heat dissipation is small. Therefore, increasing a board's thickness reduces the thermal resistance. If the copper foil area is large, since the vertical thermal conduction takes precedence, decreasing the board thickness reduces the thermal resistance. The boundary between the two situations depends on the PCB conditions.

Number of layers

- The thermal resistance tends to be lower when the number of layers is increased. However, in the multi-layer boards, the thermal resistance can be efficiently lowered by placing a larger copper foil area for heat dissipation on the same layer as the heat source or the adjacent layer.

Copper foil thickness

- The thicker the copper foil, the lower the thermal resistance. The effect is more significant when the copper foil area is larger.

Thermal via

- The larger the number of vias, the lower the thermal resistance. However, since the effect is reduced if the vias are separated farther from the heat source, place the vias near the heat source.
- The larger the via diameter, the lower the thermal resistance. However, care must be taken when placing the vias, because solder is more likely to be sucked into the vias during the reflow process if the via diameter is 0.3 mm or more.

Position of heat source

- Since there are many parts, it is difficult to secure a large copper foil area for one heat source. However, intentionally lay out the heat source on the center so that the copper foil area can be evenly secured around 360°.

Neighboring heat sources

- If multiple heat sources are closely placed, the thermal interference phenomenon when all the heat sources are operated simultaneously should be considered in designing.

Distributed heat sources

- Distribution of the heat sources (power loss) is an effective measure to decrease the temperature of each device.

Consideration of passive components vulnerable to high temperature

- A layout focusing only on the electrical characteristics may cause a thermal issue.
- It is necessary to consider the positional relation of the devices that act as heat sources and the devices vulnerable to high temperature.
- If a device that acts as a heat source is placed near a device vulnerable to high temperature, keep the wiring width to the minimum necessary in order to prevent the thermal conduction through the copper wiring with a low thermal resistance.

Temperature increase of copper wiring

- For a conductor (copper foil wiring) through which a large current flows, it is necessary to determine the minimum width and thickness based on the required current capacity and the maximum tolerance for increase in the conductor temperature. Neglecting this may cause the temperature increase, deteriorating the PCB or increasing the ambient temperature.

Challenges

There are various types of power circuits. For a quiet circuit, such as a linear regulator (LDO), in which the power does not vary frequently, the PCB layout can be considered while focusing only on the heat dissipation performance. In contrast, for a circuit such as a switching regulator, in which the power varies rapidly, the EMI must also be considered in addition to the heat dissipation. There are only a few layouts capable of managing both heat dissipation and the EMI. In most cases, a point of compromise between them must be found to design the layout.

The thermal design requires a larger copper foil area. However, many countermeasures against the EMI are available based on the frequency band where the countermeasures are taken, such as using the capacitance between layers and securing the path for return current. Furthermore, these countermeasures tend to be applicable on a case-by-case (cut-and-try) basis. Therefore, it is difficult to provide a guide for all PCB. If available, refer to the guides for individual PCB.

References

[1] JESD51-3:1996, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, JEDEC Solid State Technology Association

[2] JESD51-5:1999, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*, JEDEC Solid State Technology Association

[3] JESD51-7:1999, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, JEDEC Solid State Technology Association

[4] IPC-2221A: May 2003, *Generic Standard on Printed Board Design*, IPC - Association Connecting Electronics Industries

Related application notes

[1] TO252 Package Thermal Resistance Information

[2] HTSOP-J8 Package Thermal Resistance Information (A)

[3] HTSOP-J8 Package Thermal Resistance Information (S)

Pay attention to applicable item numbers

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